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EXAMINER	
BOKHARI, SYED M	

ART UNIT	PAPER NUMBER
2473	

NOTIFICATION DATE	DELIVERY MODE
10/28/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@techlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/713,586	BAKSHI ET AL.	
	Examiner	Art Unit	
	SYED M. BOKHARI	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-22,24,25 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-22,24,25 and 27-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 30-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claim 30, it lacks the proper form for a claim directed to computer/machine readable instructions. To be statutory claims directed to computer/machine readable instructions must be embodied on a computer readable medium encoded with a process or data structure usable by a computer. For the claim to be statutory the preamble of the claim must define a structural and functional interrelationship between the process or data structure and computer software and hardware components. As a result, the preamble of the claim must define a process or data structure as "a non- transitory machine readable medium encoded with instructions" embodying the process or data structure.

Claims 31-34 are also rejected as the claimed invention is directed to non-statutory subject matter as described above.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy et al. (US 2003/0223425 A1) in view of Hartmann et al. (US 5,936,957) and further in view of Markham (US 2003/0126468 A1).

Shenoy et al. discloses a communication system for distributed implementation of control protocols in routers and switches with the following features: regarding claim 1, a system, comprising a control card, comprising (Fig.1, distributed processing architecture, see "network node includes a control module 106" recited in paragraph 0016 lines 3-4), a control processor to execute a control portion of an exterior gateway protocol (Fig.1, distributed processing architecture, see "control module 106 and 108 include a processor 122 to carry out the function" recited in paragraph 0018 lines 1-3), a routing table of exterior gateway routes and devices (Fig.1, distributed processing architecture, see "updating forwarding information, programming hardware tables" recited in paragraph 0017 lines 4-9), a line card, comprising (Fig.1, distributed processing architecture, see "three line cards 102A, 102B and 102C" recited in paragraph 0016 lines 5-6), a line processor to execute an offload portion of an exterior gateway protocol (Fig.1, distributed processing architecture, see "line processor 118 performs functions" recited in paragraph 0020 lines 10-12) and a communications port to allow termination of at least one communication link (Fig.1, distributed processing architecture, see "each line card includes at least one port to allow link termination" recited in paragraph 0020 lines 1-6); regarding claim 3, the control processor further comprising an Intel Architecture processor (Fig.1, distributed processing architecture, see "processor within each control module includes Intel1386 processor family" recited in paragraph 0018 lines 1-5); regarding claim 5, the line processor further comprising an Intel IXP processor (Fig.1, distributed processing architecture, see "processor within

each control module includes Intel1386 processor family" recited in paragraph 0018 lines 1-5).

Shenoy et al. do not disclose the following features: regarding claim 1, backplane to allow the control card and the line card to communicate and wherein the line card is configured to filter all malformed, illegal and duplicate update messages from peer gateway peers; regarding claim 2, the control processor further comprising a general-purpose processor; regarding claim 4, the line processor further comprising a network-enabled processor; regarding claim 6, the backplane further comprising a physical backplane connection and regarding claim 7, the backplane further comprising a network.

Hartmann et al. disclose a communication system for providing a structure of ATM communication system with the following features: regarding claim 1, backplane to allow the control card and the line card to communicate (Fig. 1, shows the structure of an ATM communication system with a modular structure, see "the communication adapter is formed by a line module, realizing an ATM subscriber connection and an EISA control module realizing an EISA bus connection" recited in column 3 lines 53-60); regarding claim 2, the control processor further comprising a general-purpose processor (Fig. 1, shows the structure of an ATM communication system with a modular structure, see "a personal computer is realized by commercially available personal compute" recited in column 5 lines 33-48); regarding claim 4, the line processor further comprising a network-enabled processor (Fig. 1, shows the structure of an ATM communication system with a modular structure, see "a processor controlled

communication" recited in column 2 lines 24-35); regarding claim 6, the backplane further comprising a physical backplane connection (Fig. 1, shows the structure of an ATM communication system with a modular structure, see "the communication adapter is formed by a line module, realizing an ATM subscriber connection and an EISA control module realizing an EISA bus connection" recited in column 3 lines 53-60) and regarding claim 7, the backplane further comprising a network (Fig. 1, shows the structure of an ATM communication system with a modular structure, see "user network interface" recited in column 4 lines 57-67) and registering a control portion of a protocol to be executed by the control card with a central registration point (Fig.3, flow of a control protocol for distributed implementation of OSPF control protocol, see "offload portion of distributed control protocol is forwarded of the router 12 to control plane" recited in paragraph 0021 lines 1-27).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Shenoy et al. by using the features, as taught by with Hartmann et al., in order to provide backplane to allow the control card and the line card to communicate and wherein the line card is configured to filter all malformed, illegal and duplicate update messages from peer gateway peers, the control processor further comprising a general-purpose processor, the line processor further comprising a network-enabled processor, the backplane further comprising a physical backplane connection and the backplane further comprising a network. The motivation of using these functionalities is that it discloses a communication system for providing a structure of ATM communication system.

Shenoy et al. and Hartmann et al. do not disclose the following features: regarding claim 1, wherein the line card is configured to filter all malformed, illegal and duplicate update messages from peer gateway peers.

Markham discloses a system and method for restricting packet transfer to a computer across a network, wherein the computer includes a network interface device coupled to the network and wherein the network interface device includes a packet filter wherein a security server is connected to the network and we a packet is received at the network interface device and the network interface device determines if the packet is an authorized transaction with the following features: regarding claim 1, wherein the line card is configured to filter all malformed, illegal and duplicate update messages from gateway peers (Fig.1, illustrates various embodiment of a distributed firewall system, see "NIC 14 implements IPSEC, packet filtering, Intrusion detection etc. and replication capability" " recited in paragraph 0065 lines 1-7 and paragraph 0117 lines 1-10);

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Shenoy et al. with Hartmann et al. by using the features, as taught by Markham in order to provide the line card is configured to filter all malformed, illegal and duplicate update messages from gateway peers. The motivation of using these functions is that it discloses a system and method for restricting packet transfer to a computer across a network, wherein the computer includes a network interface device coupled to the network and wherein the network interface device includes a packet filter wherein a security server is connected to the

network and we a packet is received at the network interface device and the network interface device determines if the packet is an authorized transaction.

6. Claims 8, 10-14, 17-18, 25 and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy et al. (US 2003/0223425 A1) in view of Moberg et al. (USP 6,697,872) and further in view of Li (US 7,233,567 B1).

Shenoy et al. discloses a communication system for distributed implementation of control protocols in routers and switches with the following features: regarding claim 8, a method of processing an exterior gateway protocol packet (Fig.1, distributed processing architecture, see "protocols are implemented by control module" recited in paragraph 0017 lines 9-16), receiving an incoming packet at a line-card (Fig.1, distributed processing architecture, see "line cards receive the traffic" recited in paragraph 0020 lines 1-4), Parsing the packet to extract protocol data (Fig.1, distributed processing architecture, see "packet parsing" recited in paragraph 0020 lines 10-12); transmitting any control-relevant data to a control card (Fig.3 line card operating system, see "forwarding information to control module" recited in paragraph 0035 lines 1-7); regarding claim 13, transmitting any control-relevant data to a control card (Fig. 2, router implementing a distributed control protocol, see "line card operating system communicates with control module" recited in paragraph 0027 lines 1-8) and further comprising transmitting data related to valid updates from the peer gateways (Fig.1, distributed processing architecture, see "protocols are implemented by control module"

recited in paragraph 0017 lines 9-16); regarding claim 25, a method of establishing a control portion of a distributed exterior gateway protocol (Fig.4, flow diagram of a process for implementing the distributed, see "perform the offload portion of the of the distributed control protocol" recited in paragraph 0032 lines 10-17), executing offload portions of the protocol (Fig.1, distributed processing architecture, see "control module 106 and 108 include a processor 122 to carry out the function" recited in paragraph 0018 lines 1-3), registering a control portion of a protocol to be executed by the control card with a central registration point (Fig.1, distributed processing architecture, see "line processor 118 performs functions" recited in paragraph 0020 lines 10-12), setup a control connection with a control card (Fig. 2, router implementing a distributed control protocol, see "TCP includes set up control" recited in paragraph 0028 lines 5-7), setting up control connections with line-cards (Fig. 2, router implementing a distributed control protocol, see "TCP includes set up control" recited in paragraph 0028 lines 5-7), and performing central Border Gateway Protocol functions (Fig.1, distributed processing architecture, see "control module implements border gateway protocol BGP" recited in paragraph 0017 lines 9-16); regarding claim 27, registering a control portion of a protocol to be executed further comprising registering the control portion with a distributed control plane architecture infrastructure module (Fig.3, depicts a system for distributing forwarding information through a user space and kernel space, see "distribution engine manages the distribution of forwarding information at kernel space level" recited in paragraph 0032 lines 4-15); Regarding claim 28, performing central Border Gateway Protocol functions further comprising processing valid updates from the

line cards and adjusting the routing table as needed (Fig.3, depicts a system for distributing forwarding information through a user space and kernel space, see "the forwarding tables in the user space and kernel space are updated" recited in paragraph 0034 lines 20-26); regarding claim 29, performing central Border Gateway Protocol functions further comprising providing an updated routing table to each line card as necessary (Fig.1, distributed processing architecture, see "the distribution of forwarding information between control module and line cards has a distributed processing architecture" recited in paragraph 0031 lines 1-19); regarding claims 30, an article of machine-readable code containing instructions that, when executed, cause the machine to (Fig.1, distributed processing architecture, see "to execute a sequence of machine-readable instructions" recited in paragraph 0046 lines 1-10), receiving an incoming packet at a line-card (Fig.1, distributed processing architecture, see "line cards receive the traffic" recited in paragraph 0020 lines 1-4), Parsing the packet to extract protocol data (Fig.1, distributed processing architecture, see "packet parsing" recited in paragraph 0020 lines 10-12) and transmitting any control-relevant data to a control card (Fig.3 line card operating system, see "forwarding information to control module" recited in paragraph 0035 lines 1-7); regarding claim 31, the instructions causing the machine to receive an incoming packet at a line-card (Fig.1, distributed processing architecture, see "line cards receive the traffic" recited in paragraph 0020 lines 1-4), further cause the machine to receive a packet through the Transmission Control Protocol (Fig.2, two communication channel used to communicate information, see "uses reliable transport layer protocol TCP" recited in paragraph 0028 lines 3-7).

Shenoy et al. do not disclose the following features: regarding claim 8, determining if the packet is valid and generating message traffic at the line card for peer gateways including announcing routes to the peer gateways; regarding claim 10, determining if the packet is valid further comprising determining if the packet is a malformed packet; regarding claim 11, if the packet is valid further comprising applying a packet filter to the packets; regarding claim 12, determining if the packet is valid further comprising applying an address filter to the packets; regarding claim 14, further comprising decrypting encrypted packets; regarding claim 17, generating message traffic for peer gateways further comprising encrypting messages for peer gateways that require encryption; regarding claim 25, initializing a control card, configuring the line card, including providing a routing table and policy data to each line card; regarding claim 30, determining if the packet is valid and generate message traffic for peer gateways including announcing routes to the peer gateways; regarding claim 32, the instructions causing the machine to determine if the packet is valid further causes the machine to determine if the packet is a mal-formed packet; regarding claim 33, the instructions causing the machine to determine if the packet is valid further causes the machine to apply a packet filter to the packet and regarding claim 34, the instructions causing the machine to determine if the packet is valid further causes the machine to apply an address filter to the packet.

Moberg et al. discloses a communication system for distributed packet processing using encapsulation and decapsulation chains with the following features: regarding claim 8, determining if the packet is valid (Fig.1, distributed processing

architecture, see "examine the entire packet to verify its validity" recited in column 4 lines 55-58); regarding claim 10, determining if the packet is valid further comprising applying a packet filter to the packets (Fig.1, distributed processing architecture, see "examine the entire packet to verify its validity" recited in column 4 lines 55-62); regarding claim 11, if the packet is valid further comprising applying a packet filter to the packets (Fig.1, distributed processing architecture, see "after validation the data packet processed" recited in column 4 lines 47-49); regarding claim 12, determining if the packet is valid further comprising applying an address filter to the packets (Fig.1, distributed processing architecture, see "examine the network address of the received packet" recited in column 4 lines 49-51); regarding claim 14, further comprising decrypting encrypted packets (Fig. 4, chain walker used to process packet, see "decryption element 60" recited in column 7 lines 10-16); regarding claim 17, generating message traffic for peer gateways further comprising encrypting messages for peer gateways that require encryption (Fig. 4, chain walker used to process packet, see "the chain includes an encryption element 74" recited in column 7 lines 10-16 and lines 25-28); regarding claim 25, initializing a control card (Fig.1, distributed processing architecture, see "building chains on the router processor and line card upon initialization or configuration change" recited in column 7 lines 60-67 and column 8 lines 1-5); regarding claim 30, determining if the packet is valid (Fig.1, distributed processing architecture, see "examine the entire packet to verify its validity" recited in column 4 lines 55-58); regarding claim 32, the instructions causing the machine to determine if the packet is valid further causes the machine to determine if the packet is a mal-formed

packet (Fig.1, distributed processing architecture, see "examine the entire packet to verify its validity" recited in column 4 lines 55-62); regarding claim 33, the instructions causing the machine to determine if the packet is valid further causes the machine to apply a packet filter to the packet (Fig.1, distributed processing architecture, see "after validation the data packet processed" recited in column 4 lines 47-49); regarding claim 34, the instructions causing the machine to determine if the packet is valid further causes the machine to apply an address filter to the packet (Fig.1, distributed processing architecture, see "examine the network address of the received packet" recited in column 4 lines 49-51).

Shenoy et al. and Moberg et al. do not fully disclose the following features: regarding claim 8, generating message traffic at the line card for peer gateways including announcing routes to the peer gateways; regarding claim 25, configuring the line card, including providing a routing table and policy data to each line card; regarding claim 30, generate message traffic for peer gateways including announcing routes to the peer gateways;

Li discloses an apparatus and method for managing multiple traffic redundancy mechanisms includes a resource manager for managing the multiple redundancy mechanisms for bridging traffic between a working port and a protection port, and uses an agent for the working port in order to maintain routes associated with the working port even after a failure occurs that affects communication over the working port with the following features: regarding claim 8, generating message traffic at the line card for peer gateways including announcing routes to the peer gateways (Fig. 3, a block

diagram showing the relevant components of an exemplary line card in accordance with an embodiment of the present invention, see "The RSP memory 330 is used to store the routing table. The core processor 310 provides management and control for the line card 130, and includes logic for receiving the routing table from the central controller 120 over the fast bus, storing the routing table in the RSP memory 330, and configuring the RSP 320 based upon predetermined configuration information" recited in column 5 lines 1-19); regarding claim 25, configuring the line card, including providing a routing table and policy data to each line card (Fig. 3, a block diagram showing the relevant components of an exemplary line card in accordance with an embodiment of the present invention, see "The RSP memory 330 is used to store the routing table. The core processor 310 provides management and control for the line card 130, and includes logic for receiving the routing table from the central controller 120 over the fast bus, storing the routing table in the RSP memory 330, and configuring the RSP 320 based upon predetermined configuration information" recited in column 5 lines 1-19); regarding claim 30, generate message traffic for peer gateways including announcing routes to the peer gateways (Fig. 3, a block diagram showing the relevant components of an exemplary line card in accordance with an embodiment of the present invention, see "The RSP memory 330 is used to store the routing table. The core processor 310 provides management and control for the line card 130, and includes logic for receiving the routing table from the central controller 120 over the fast bus, storing the routing table in the RSP memory 330, and

configuring the RSP 320 based upon predetermined configuration information" recited in column 5 lines 1-19);

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Shenoy et al. with Moberg et al. by using the features, as taught by Li, in order to provide generating message traffic at the line card for peer gateways including announcing routes to the peer gateways, configuring the line card, including providing a routing table and policy data to each line card. The motivation of using these functions is that it discloses an apparatus and method for managing multiple traffic redundancy mechanisms includes a resource manager for managing the multiple redundancy mechanisms for bridging traffic between a working port and a protection port, and uses an agent for the working port in order to maintain routes associated with the working port even after a failure occurs that affects communication over the working port.

7. Claims 18-22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy et al. (US 2003/0223425 A1) in view of Moberg et al. (USP 6,697,872) and Li (US 7,233,567 B1) and further in view of Ball et al. (US 2005/0074003 A1).

Shenoy et al. disclose the following features: regarding claim 18, a method of establishing an offload portion of a distributed exterior gateway protocol comprising (Fig.1, distributed processing architecture, see "line processor 118 performs functions" recited in paragraph 0020 lines 10-12), registering an offload portion of a protocol to be

executed by the line-card with a central registration point (Fig.1, distributed processing architecture, see "line processor 118 performs functions" recited in paragraph 0020 lines 10-12), setup a control connection with a control card (Fig. 2, router implementing a distributed control protocol, see "TCP includes set up control" recited in paragraph 0028 lines 5-7); transmit data resource data to the control card (Fig.3 line card operating system, see "forwarding information to control module" recited in paragraph 0035 lines 1-7); receiving configuration information from the control card (Fig.1, distributed processing architecture, see "control module implement configuration commands" recited in paragraph 0017 lines 1-6), performing Border Gateway Protocol functions at the line-card (Fig. 2, router implementing a distributed control protocol, see "TCP includes set up control" recited in paragraph 0028 lines 5-7), and performing central Border Gateway Protocol functions (Fig.1, distributed processing architecture, see "control module implements border gateway protocol BGP" recited in paragraph 0017 lines 9-16) and transmitting only valid Border Gateway Protocol data to the control card (Fig.1, distributed processing architecture, see "protocols are implemented by control module" recited in paragraph 0017 lines 9-16); regarding claim 19, registering an offload portion further comprising registering with a distributed control plane architecture infrastructure module (Fig.3, flow of a control protocol for distributed implementation of OSPF control protocol, see "offload portion of distributed control protocol is forwarded of the router 12 to control plane" recited in paragraph 0021 lines 1-27) regarding claim 20, performing Border Gateway Protocol functions (Fig.1, distributed processing architecture, see "control module implements border gateway protocol BGP" recited in

paragraph 0017 lines 9-16) and further comprising parsing and validating incoming packets (Fig.1, distributed processing architecture, see "the processor performs packet parsing" recited in paragraph 0020 lines 10-12); regarding claim 22, performing Border Gateway Protocol functions (Fig.1, distributed processing architecture, see "control module implements border gateway protocol BGP" recited in paragraph 0017 lines 9-16) and further comprising caching a routing table received from the control card (Fig.1, distributed processing architecture, see "the control module send the forwarding information" recited in paragraph 0017 lines 1-16); regarding claim 24, performing Border Gateway Protocol functions (Fig.1, distributed processing architecture, see "control module implements border gateway protocol BGP" recited in paragraph 0017 lines 9-16);

Moberg et al. disclose the following features: regarding claim 18, initializing a line card (Fig.1, distributed processing architecture, see "building chains on the router processor and line card upon initialization or configuration change" recited in column 7 lines 60-67 and column 8 lines 1-5); regarding claim 21, performing Border Gateway Protocol functions further comprising filtering all malformed, illegal and duplicate update messages from gateways peers (Fig.1, distributed processing architecture, see "examine the entire packet to verify its validity and determine how to handle" recited in column 4 lines 43-67) regarding claim 24, further comprising encrypting and decrypting packets as necessary (Fig. 4, chain walker used to process packet, see "decryption element 60" recited in column 7 lines 10-16 and lines 25-28);

Li discloses the following features: regarding claim 18, performing Border Gateway Protocol functions at the line-card, including running output policies for the each of the gateway peers (Fig. 3, a block diagram showing the relevant components of an exemplary line card in accordance with an embodiment of the present invention, see "The RSP memory 330 is used to store the routing table. The core processor 310 provides management and control for the line card 130, and includes logic for receiving the routing table from the central controller 120 over the fast bus, storing the routing table in the RSP memory 330, and configuring the RSP 320 based upon predetermined configuration information" recited in column 5 lines 1-19).

Shenoy et al., Moberg et al. and Li do not disclose the following features: regarding claim 18, establishing connections with exterior gateway peers.

Ball et al. disclose a communications network for implementation of efficient and scaleable routing protocol with the following features: regarding claim 18, establishing connections with exterior gateway peers (Fig. 1, in a schematic block diagram of an inter-domain router, see "establish a logical peer connection" paragraph 0004 lines 1-13 in the background of the invention) and including running output policies for the each of the gateway peers (Fig. 6, an schematic block diagram illustrating the BGP protocol, see "the BGP running inbound policy on all routes" recited in paragraph 0041 lines 1-17).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Shenoy et al. with Moberg et al. and by using the features, as taught by Ball et al., in order to provide establishing connections with

exterior gateway peers and including running output policies for the each of the gateway peers. The motivation of using these functions is that it discloses a communications network for implementation of efficient and scaleable routing protocol.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy et al. (US 2003/0223425 A1) in view of Moberg et al. (USP 6,697,872) and Li (US 7,233,567 B1) as applied to claim 8 above, and further in view of Harvey et al. (US 2003/0140167 A1).

Shenoy et al., Moberg et al. and Li disclose the claimed limitations as described in paragraph 5 above. Shenoy et al., Moberg et al. and Li do not disclose the following features: regarding claim 15, generating message traffic for peer gateways and further comprising generating responses required by the incoming packets.

Harvey et al. discloses a method and apparatus for synchronizing redundant communication task with the following features: regarding claim 15, generating message traffic for peer gateways (Fig. 1, flow chart depicting a method for synchronizing TCP tasks, see "an update message should be generated" recited in paragraph 0032 lines 1-11) and further comprising generating responses required by the incoming packets (Fig. 1, flow chart depicting a method for synchronizing TCP tasks, see "issuing TCP packet acknowledgement message step 126" recited in paragraph 0030 lines 1-10).

It would have been obvious to one of the ordinary skill in the art at the time of the

invention to modify the system of Shenoy et al. with Moberg et al. and Li by using the features, as taught by Harvey et al., in order to provide of generating message traffic for peer gateways and further comprising generating responses required by the incoming packets. The motivation of using this functionality is that it discloses a method and apparatus for synchronizing redundant communication task.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SYED M. BOKHARI whose telephone number is (571)270-3115. The examiner can normally be reached on Monday through Friday 8:00-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang B. Yao can be reached on 5712723182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SYED M BOKHARI/
Examiner, Art Unit 2473
10/18/2010

/KWANG B. YAO/
Supervisory Patent Examiner, Art Unit 2473